TTool/DIPLODOCUS: a UML Model-Driven Environment for Embedded Systems-on-Chip Design

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1 Introduction

The hardware/software partitioning of an embedded system intends to determine how the system's functionalities are to be implemented in hardware or software. More concretely, a given functionality, such as a signal processing algorithm, can be implemented either in software - i.e., as a set of processes running on a CPU - or in hardware - i.e., via a dedicated electronic circuit.
Typically, partitioning decisions are taken according to criteria such as latency, throughput, silicon area, power consumption, etc. These criteria steer the exploration of the system's design space, where the desired hardware/software implementation is selected after evaluating different combinations of hardware and software.
Hardware/software partitioning tools and methodologies have been thoroughly studied for centralized systems (i.e., single-processor architectures). However, these tools and methodologies are more and more strained by the impact of the complex communication schemes (e.g., hierarchical bus architectures, Networks-on-Chip) that can be found in today's parallel and distributed systems (e.g., Multi-Processor Systems-on-Chip, MPSoCs).

2 The seminar

This talk focuses on the tool and methodology underlying TTool/DIPLODOCUS, that have been developed at the System-on-Chip laboratory of Telecom ParisTech during the last years of research.
TTool/DIPLODOCUS is a UML toolkit that targets the hw/sw partitioning and design space exploration of heterogeneous Systems-on-Chips dedicated to data-dominated applications (e.g., signal and video processing). More specifically, TTool is a free and open-source toolkit that supports the edition, simulation and formal verification of UML diagrams for the DIPLODOCUS UML profile.
The presentation is organized as follows:

1. The basic features of the DIPLODOCUS profile will be introduced with a focus on the modeling semantics and the abstraction level (i.e., System Level).

2. A demonstration will then show the modeling, simulation and formal verification capabilities of TTool/DIPLODOCUS by means of a sample smart-card system. The core strengths of TTool/DIPLODOCUS, such as its press-button approach, ease of use and the models' transformations, will be illustrated via the design and verification of the smart-card.
3. The talk will be concluded by a presentation of our most recent research works: the Psi-chart design methodology. The latter is an extension of the well known Y-chart design approach and is dedicated to the design of parallel and distributed SoCs. During this third section, we will motivate our works by explaining the deficiencies of the Y-chart approach when it comes to the design of parallel and distributed SoCs and their interconnect. We will then present the overall Psi-chart design approach and illustrate its implementation in TTool/DIPLODOCUS by means of a case study showing the design of the physical layer of a Software Defined Radio system.

3 Biographies

Andrea Enrici obtained his M.Sc. in Electronic Engineering from Telecom ParisTech in 2011 and from Politecnico di Torino in 2012 (summa cum laude). Since November 2012, he is a Ph.D. student in the System-on-Chip laboratory of Telecom ParisTech located at Sophia Antipolis, France, under the supervision of Ludovic Apvrille and Renaud Pacalet. His current research focuses on model driven engineering and code generation for parallel and distributed embedded Systems-on-Chip.

Dr. Ludovic Apvrille obtained his M.Sc. in Computer Science in 1998 from ENSEIRB and ISAE. He then completed a Ph.D. in 2002, in the Department of Applied Mathematics and Computer Science at ISAE, in collaboration with LAAS-CNRS and Thals Alenia Space. After a postdoctoral term at Concordia University (Canada), he joined Telecom ParisTech in 2003 as an assistant professor, in the Communication and Electronics department. He obtained his HDR (Habilitation Diriger les Recherches) in 2012. His research interests focus on tools and methods for the modeling and verification of embedded systems and Systems-on-Chip. Verification techniques target both safety and security properties. He's the leader of the open-source UML/SysML toolkit named TTool.

Pr. Renaud Pacalet received his M.S. from Telecom ParisTech in 1988. He currently leads the "Systems on Chip" laboratory of Telecom ParisTech in Sophia-Antipolis, France. His current research topics are about the hardware/software architectures of Digital Signal Processors for the Software Defined Radio, and the integrity and confidentiality of external memories of integrated systems. Some of his past research activities were also about hardware acceleration of ray tracing, hardware architectures for video coding and decoding, fault and side channel attacks against integrated circuits, countermeasures against these, intelligent transportation systems, automated driving.